

## ● HD6437043E00F (XS936A00) CPU

PLG150-DX: IC2

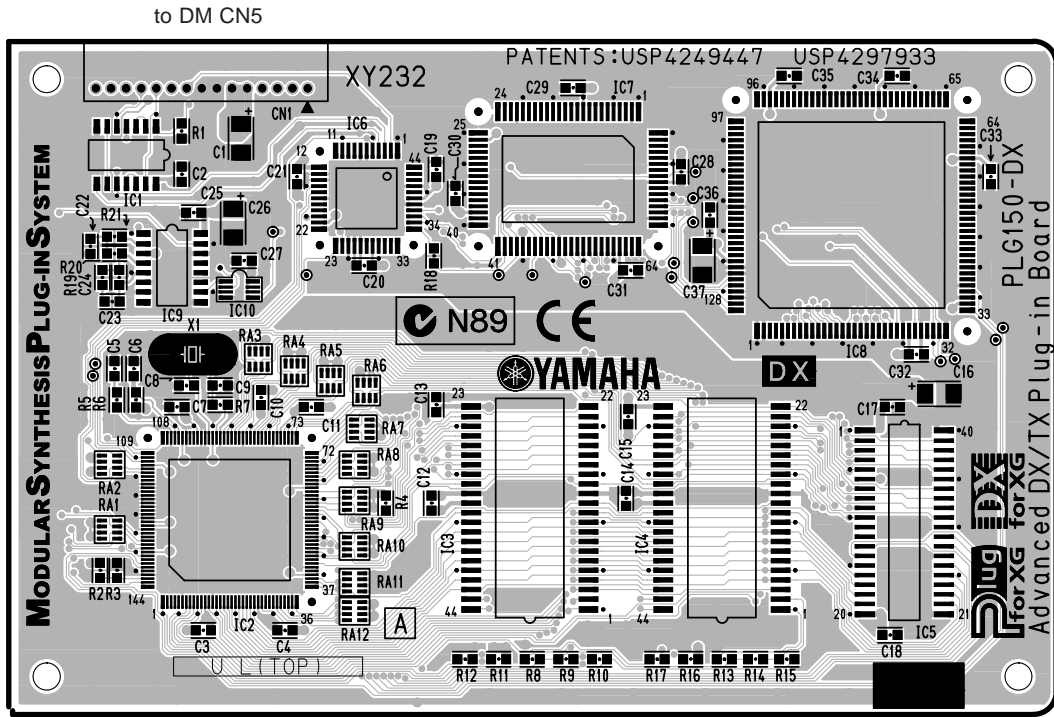
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	/WRHH	O	HH write	73	D15	I/O	Data bus	
2	DACK0	O	DMA transfer strobe	74	D14	I/O		
3	/WRHL	O	HL write	75	D13	I/O		
4	/CASHH	O	HH Column address strobe	76	D12	I/O	Power supply	
5	PE15	I/O	Port E	77	VCC	I		
6	VSS	I	Ground	78	D11	I/O		Data bus
7	A0	O	Address bus	79	VSS	I	Ground	
8	A1	O						
9	A2	O						
10	A3	O						
11	A4	O						
12	VCC	I		Power supply	80	D10	I/O	Data bus
13	A5	O	Address bus	81	D9	I/O		
14	VSS	I	Ground	82	D8	I/O		
15	A6	O	Address bus	83	D7	I/O	Power supply	
16	A7	O						
17	A8	O						
18	A9	O						
19	A10	O						
20	A11	O						
21	A12	O	Address bus	84	D6	I/O	Ground	
22	A13	O						
23	A14	O						
24	A15	O						
25	A16	O						
26	VCC	I		Power supply	85	VCC	I	Power supply
27	A17	O	Address bus	86	D5	I/O	Data bus	
28	VSS	I	Ground	87	VSS	I	Ground	
29	/CASHL	O	HL Column address strobe	88	D4	I/O	Data bus	
30	PA19	I/O	Port A	89	D3	I/O		
31	/RAS	O	Row address strobe	90	D2	I/O		
32	/CASL	O	Column address strobe (low)	91	D1	I/O	Ground	
33	PA18	I/O	Port A	92	D0	I/O		
34	/CASH	O	Column address strobe (high)	93	VSS	I		
35	VSS	I	Ground	94	XTAL	I	Crystal oscillator	
36	RDWR	O	DRAM read/write	95	MD3	I	Mode select	
37	A18	O	Address bus	96	EXTAL	I	Crystal oscillator	
38	A19	O						
39	A20	O						
40	VCC	I		Power supply	97	MD2	I	Mode select
41	A21	O		Address bus	98	NMI	-	Non-maskable interrupt
42	VSS	I		Ground	99	VCC	I	Power supply
43	/RD	O	Read	100	PA16	I/O	Port A	
44	/WDTOVF	O	Watch dog timer overflow	101	PA17	I/O	Port A	
45	D31	I/O	Data bus	102	MD1	I	Mode select	
46	D30	I/O	Data bus	103	MD0	I	Mode select	
47	/WRH	O	High write	104	PLLVCC	I	PLL Power supply	
48	/WRL	O	Low write	105	PLLCAP	I	PLL capacitor	
49	/CS1	O	Chip select	106	PLLVSS	I	PLL Ground	
50	/CS0	O	Chip select	107	PA15	I/O	Port A	
51	/IRQ3	I	Interrupt request	108	/RES	I	Reset	
52	/IRQ2	I	Interrupt request	109	/DREQ0	I	DMA transfer request	
53	/CS3	O	Chip select	110	TIOC0B	I/O	MTU input capture/output compare (ch 0)	
54	/CS2	O	Chip select	111	PE2	I/O	Port E	
55	VSS	I	Ground	112	VCC	I	Power supply	
56	D29	I/O	Data bus	113	PE3	I/O	Port E	
57	D28	I/O						
58	D27	I/O						
59	D26	I/O						
60	D25	I/O						
61	VSS	I		Ground	114	PE4	I/O	
62	D24	I/O	Data bus	115	PE5	I/O	Ground	
63	VCC	I	Power supply	116	PE6	I/O		
64	D23	I/O	Data bus	117	VSS	I		
65	D22	I/O						
66	D21	I/O						
67	D20	I/O						
68	D19	I/O						
69	D18	I/O						
70	D17	I/O	Data bus	118	AN0	I	Analog input	
71	VSS	I	Ground	119	AN1	I		
72	D16	I/O	Data bus	120	AN2	I		
				121	AN3	I	Port F	
				122	PF4	I/O		
				123	PF5	I/O		
				124	AVSS	I	Analog ground	
				125	PF6	I/O	Port F	
				126	PF7	I/O	Port F	
				127	AVREF	I	Analogreference voltage	
				128	AVCC	I	Analog power supply	
				129	VSS	I	Ground	
				130	RxD0	I	Receive data	
				131	TxD0	O	Transmit data	
				132	/IRQ1	I	Interrupt request	
				133	RxD1	I	Receive data	
				134	PA4	I/O	Port A	
				135	VCC	I	Power supply	
				136	SCK1	I/O	Serial clock	
				137	PE7	I/O	Port E	
				138	PE8	I/O		
				139	PE9	I/O		
				140	PE10	I/O	Ground	
				141	VSS	I		
				142	TIOC3D	I/O		MTU input capture/output compare (ch 3)
				143	PE12	I/O	Port E	
				144	PE13	I/O	Port E	

• YMP706-F (XT329A00) FS1-AB AWM Tone Generator & Digital Filter

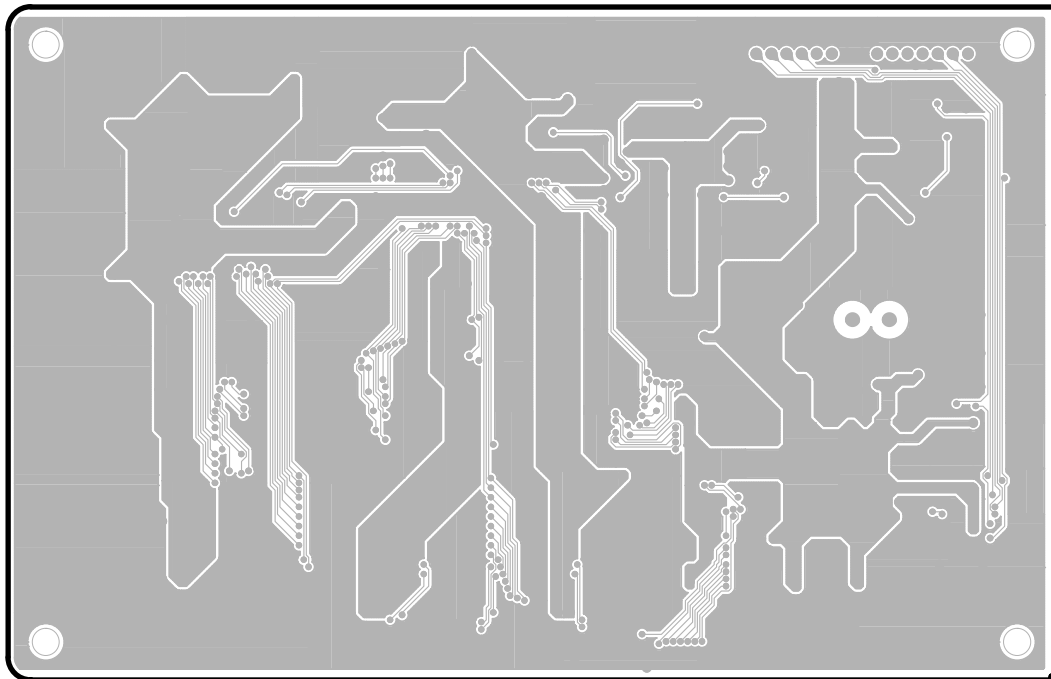
PLG150-DX: IC8

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	CHIN0	I/O	Channel data input	65	TEST	O	NC
2	CHIN1	I/O		66	TEST	O	
3	CHOUT0	O	Channel data output	67	VSS	-	Ground
4	CHOUT1	O		68	TEST	O	
5	VSS	-	Ground	69	TEST	O	NC
6	A0	I	Address input	70	TEST	O	
7	A1	I		71	TEST	O	
8	A2	I		72	TEST	O	
9	A3	I		73	TEST	O	
10	A4	I		74	TEST	O	
11	A5	I		75	TEST	O	
12	A6	I	Data input	76	VDD	-	Power supply
13	A7	I		77	TEST	O	
14	A8	I		78	TEST	O	
15	A9	I		79	TEST	O	
16	D0	I		80	TEST	O	NC
17	D1	I		81	TEST	O	
18	D2	I	Data input	82	TEST	O	Ground
19	D3	I		83	TEST	O	
20	D4	I		84	TEST	O	
21	D5	I		85	VSS	-	
22	D6	I		86	TEST	O	
23	D7	I		87	TEST	O	
24	ICL	I	Initial clear	88	TEST	O	NC
25	TSTEN	I	Test pin	89	TEST	O	
26	VDD	-	Power supply	90	TEST	O	
27	CLK	I	Clock input	91	TEST	O	
28	VSS	-	Digital ground	92	TEST	O	Power supply
29	SYWD	O	SYWD synch. signal output	93	TEST	O	
30	SYWI	I	SYW synch. signal input	94	VDD	-	
31	WEL	I	Write enable	95	TEST	I/O	NC
32	OBEN	I	Test pin	96	TEST	I/O	
33	CE0L	I	Chip enable	97	TEST	I/O	
34	CE1	I		98	TEST	I/O	
35	TSTEG	I	Test pin	99	TEST	I/O	
36	PBUSY	O	Busy output	100	TEST	I/O	
37	TMODE	I	Test pin	101	TEST	I/O	
38	HCLK	I/O	Synch. clock output	102	TEST	I/O	NC
39	SYW	I/O	SYW synch. signal output	103	TEST	I	
40	TEST	I	NC	104	TEST	I	
41	TEST	I		105	TEST	I	
42	TEST	I		106	TEST	I	
43	TEST	I		107	TEST	I	
44	TEST	I		108	TEST	I	
45	TEST	I		109	TEST	I	
46	TEST	I	Ground	110	TEST	I	
47	TEST	I		111	VSS	-	
48	TEST	I	NC	112	TEST	I	
49	VSS	-		Ground	113	TEST	I
50	TEST	I		114	TEST	I	
51	TEST	I		115	TEST	I	
52	TEST	I	NC	116	TEST	I	
53	TEST	I		117	TEST	I	
54	TEST	I		118	TEST	I	
55	TEST	I		119	TEST	I	
56	TEST	I	Power supply	120	VDD	-	
57	TEST	I		121	DIN0	I/O	
58	VDD	-	Power supply	122	DIN1	I/O	DRY input
59	TEST	O	NC	123	DOUT0	O	
60	TEST	O		124	DOUT1	O	DRY output
61	TEST	O	NC	125	SIN0	I/O	
62	TEST	O		126	SIN1	I/O	
63	TEST	O		127	SOUT0	O	SEND output
64	TEST	O		128	SOUT1	O	

• PLG150-DX Circuit Board



Component side



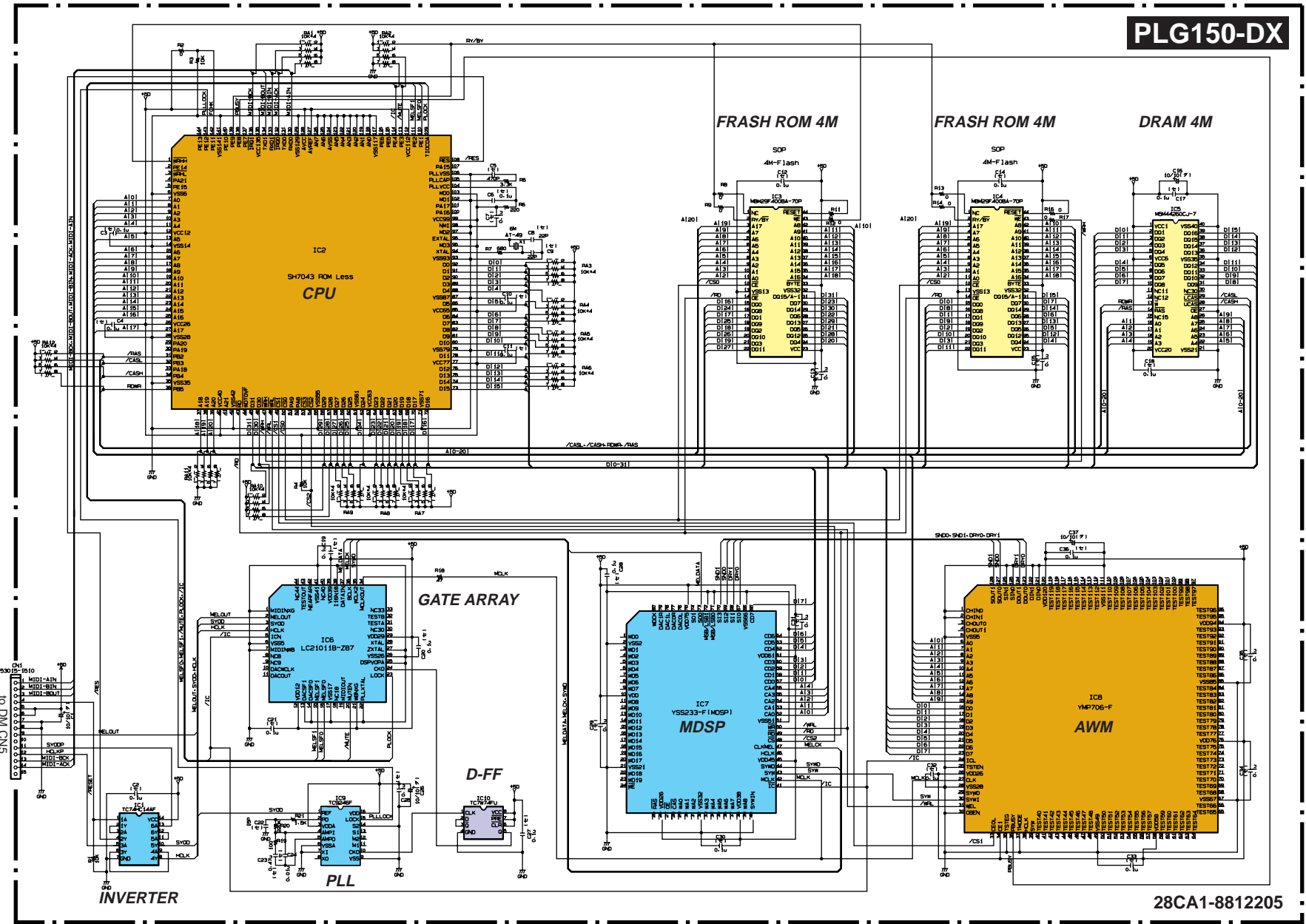
Pattern side

Note: See parts list for details of circuit board component parts.

PLG150-DX: 2NA-V414740

DX200 OVERALL CIRCUIT DIAGRAM (PLG150-DX)

PLG150-DX



28CA1-8812205